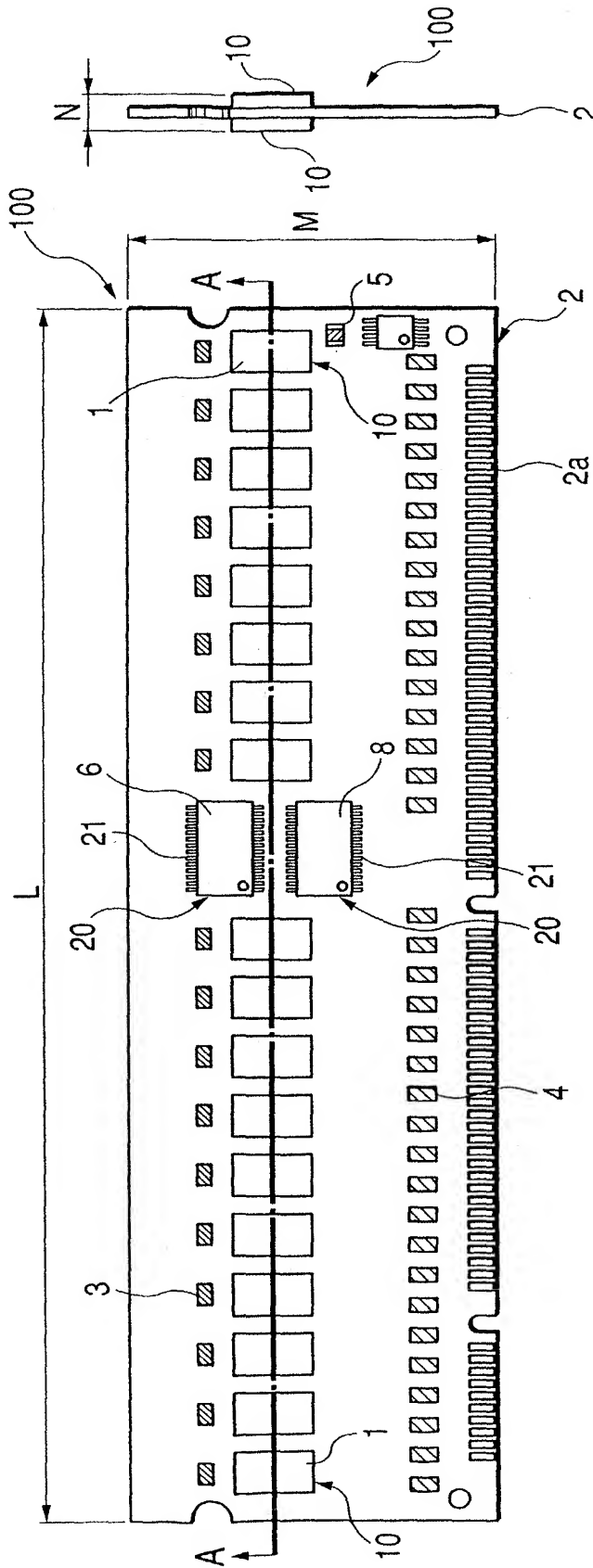


**FIG. 1(a)**



**FIG. 1(b)**

FIG. 1(c)

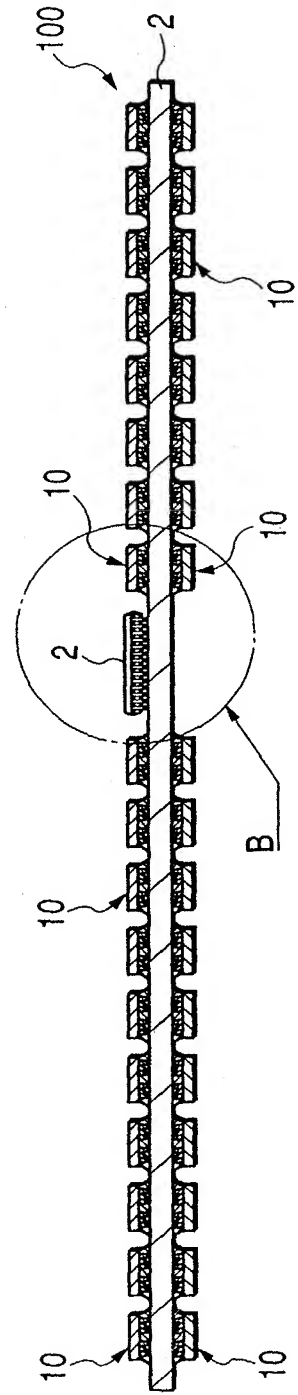
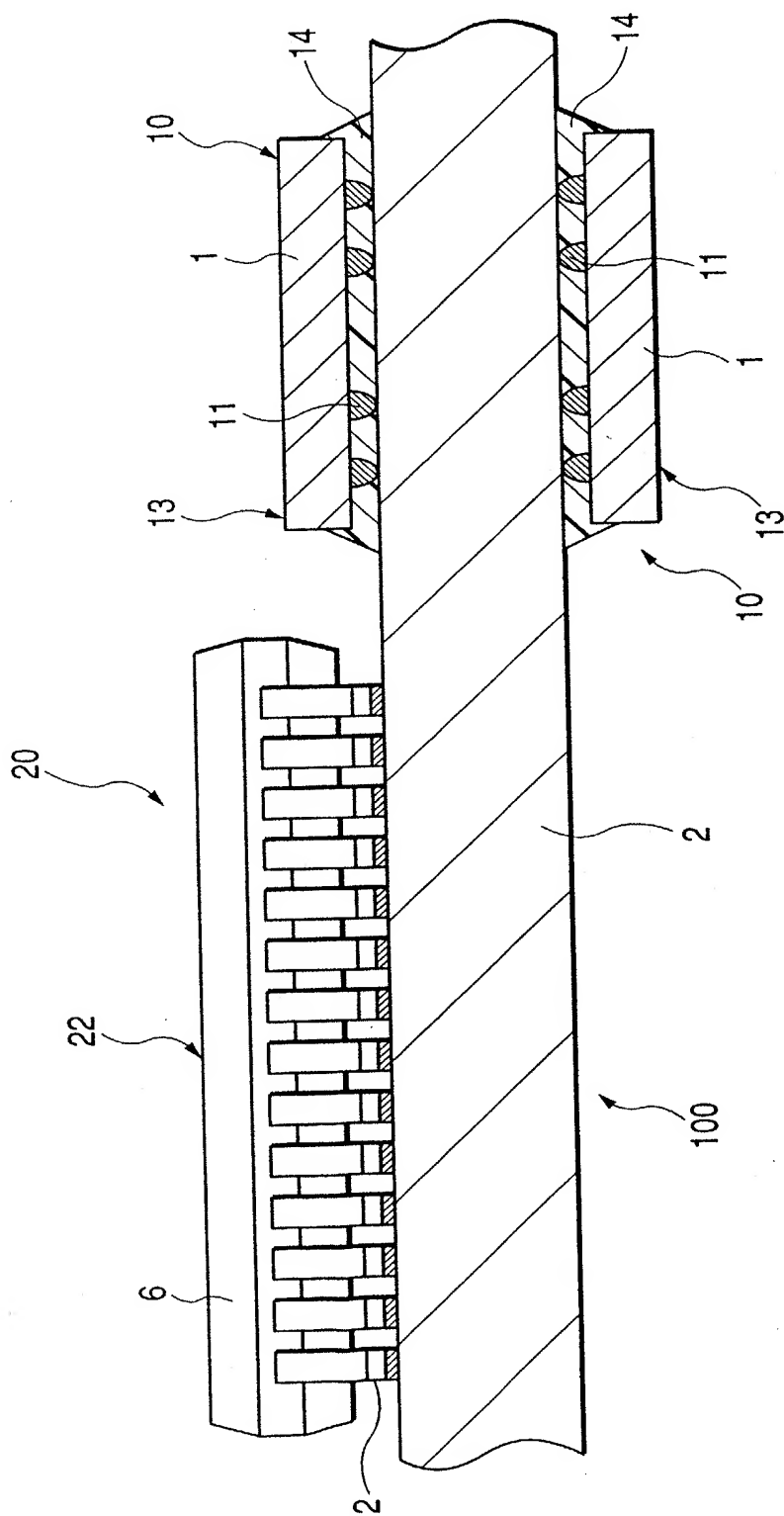


FIG. 2



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FIG. 3

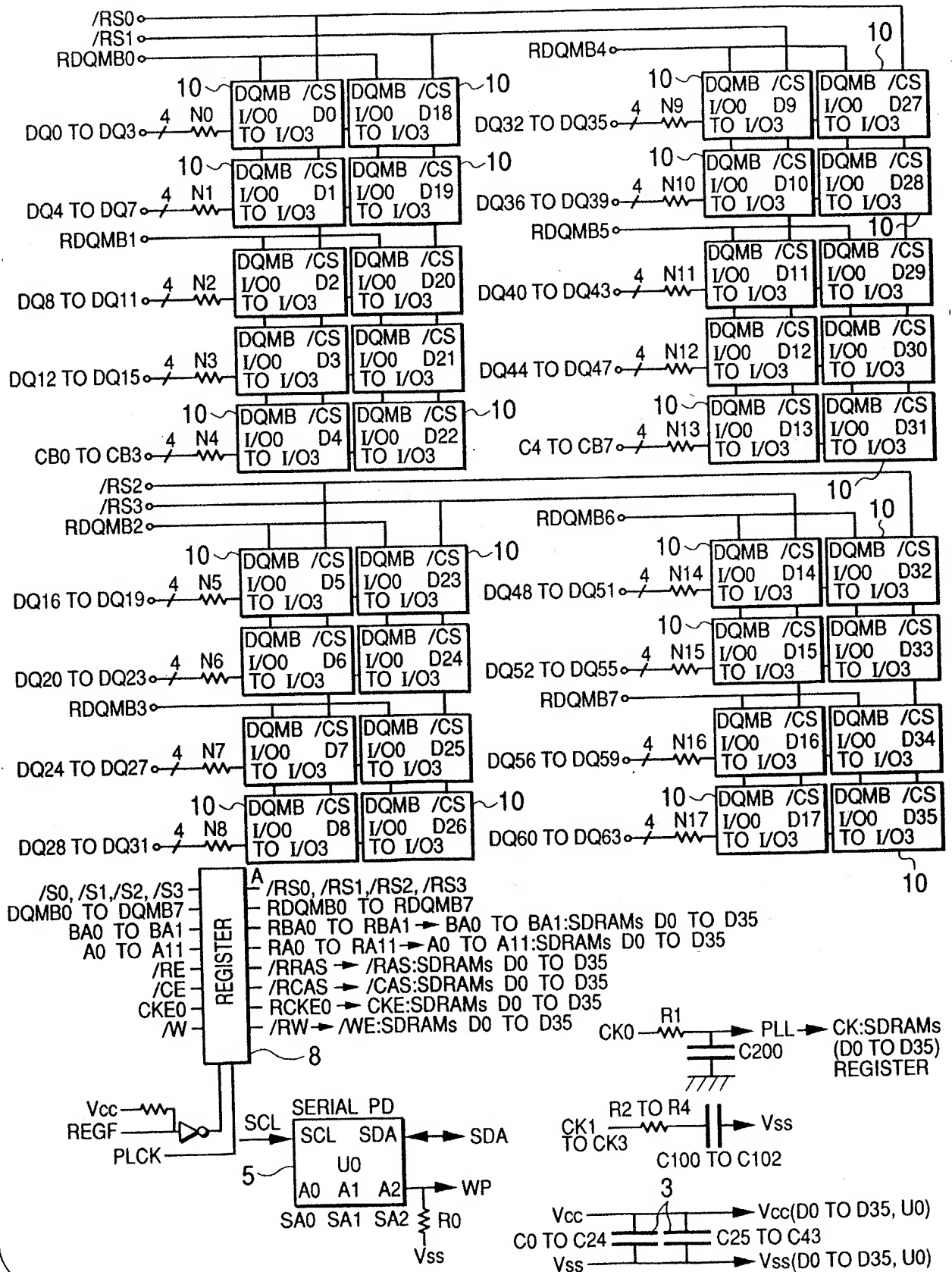


FIG. 4

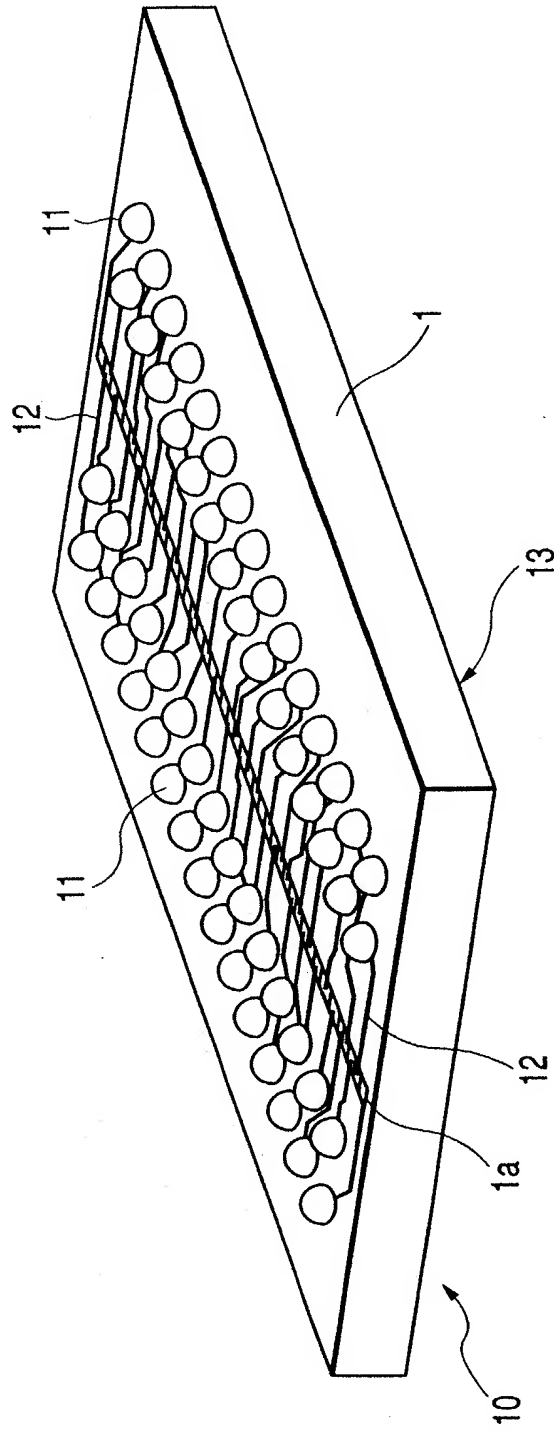


FIG. 5(a)

FIG. 5(b)

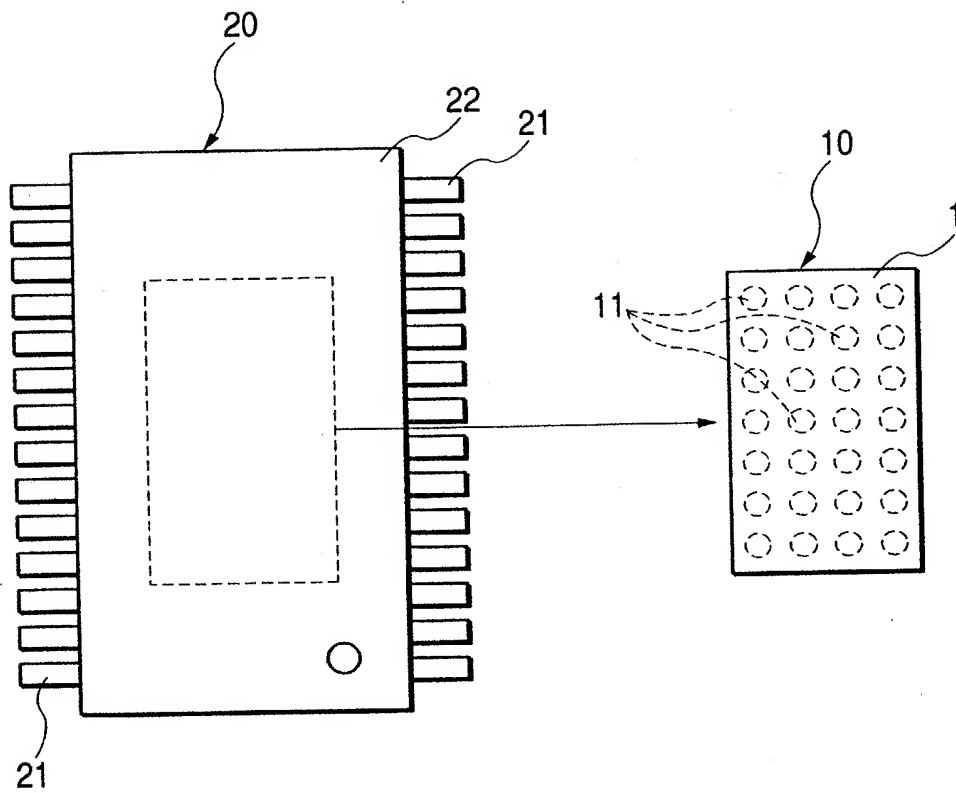
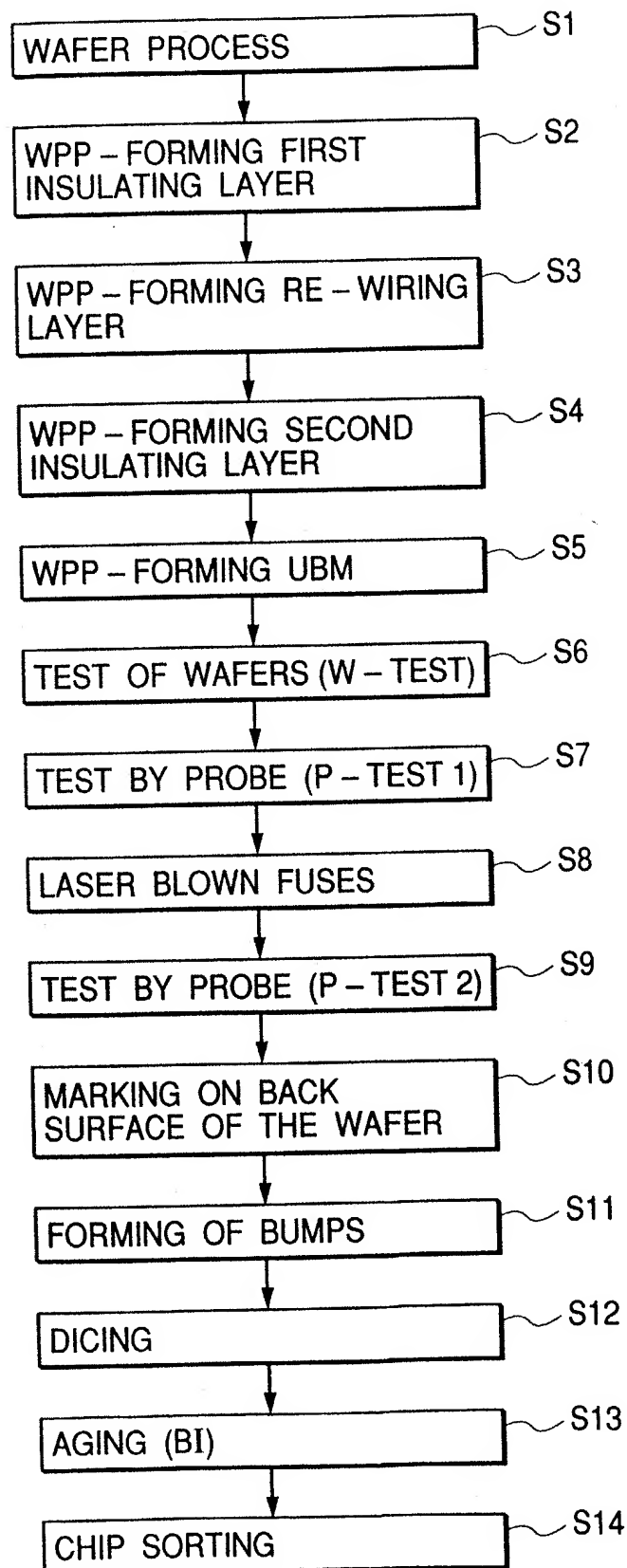
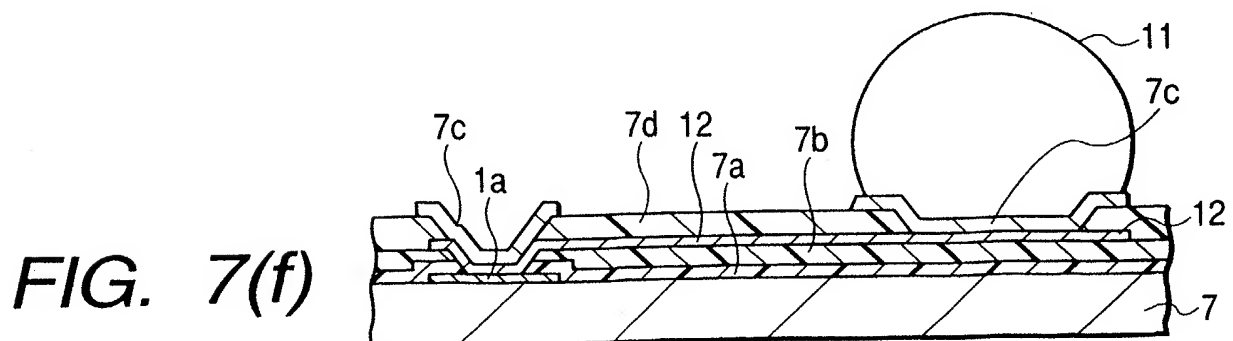
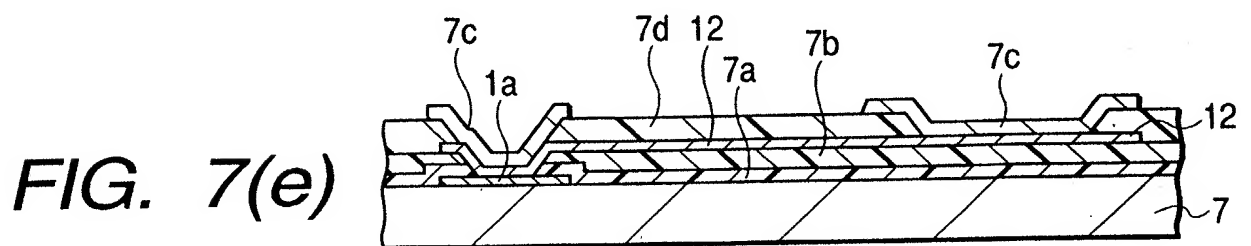
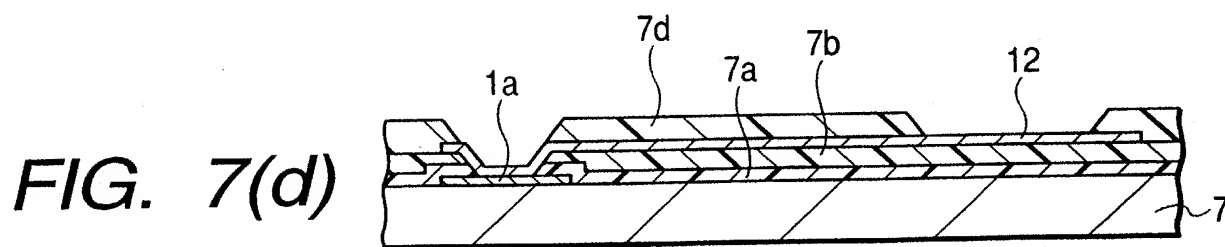
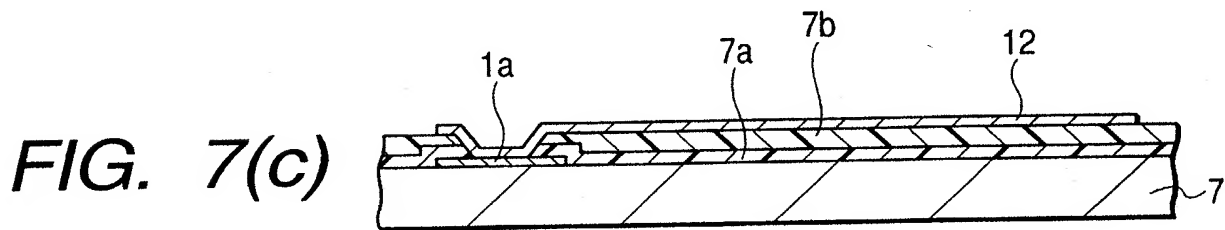
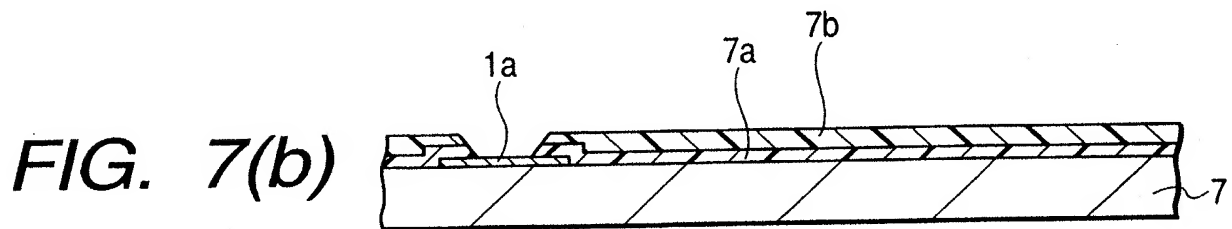
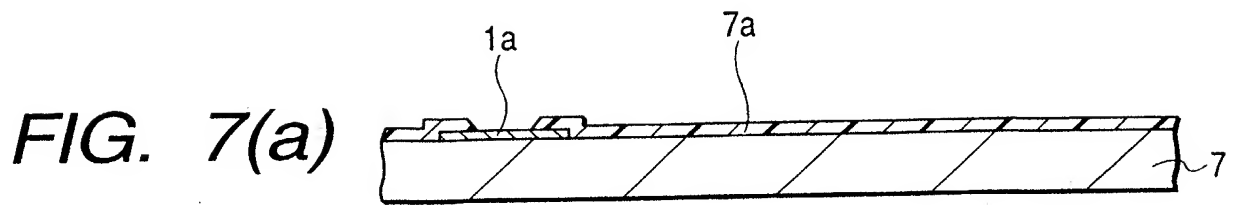


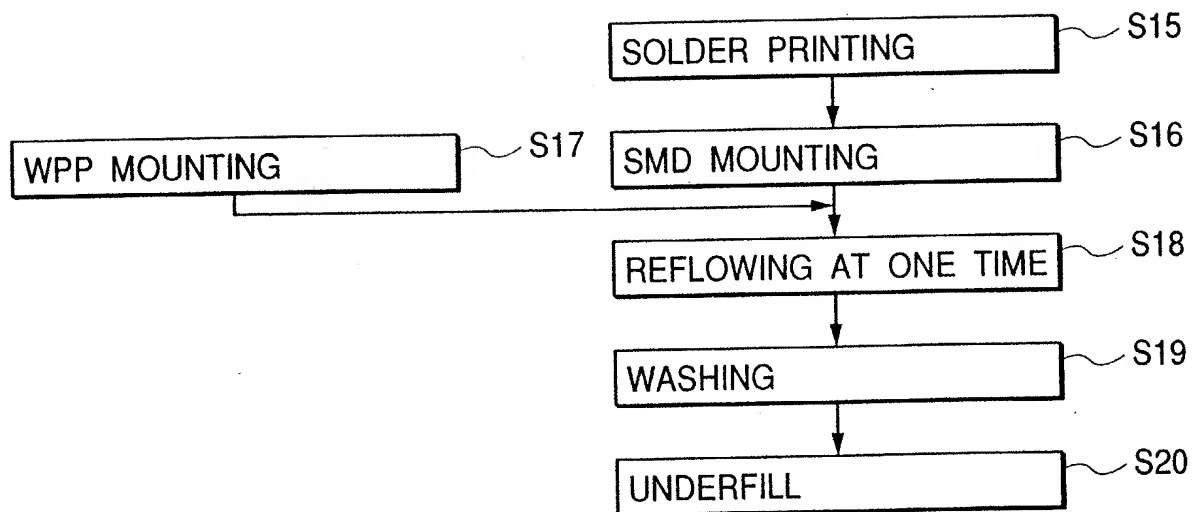
FIG. 6





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*FIG. 8*





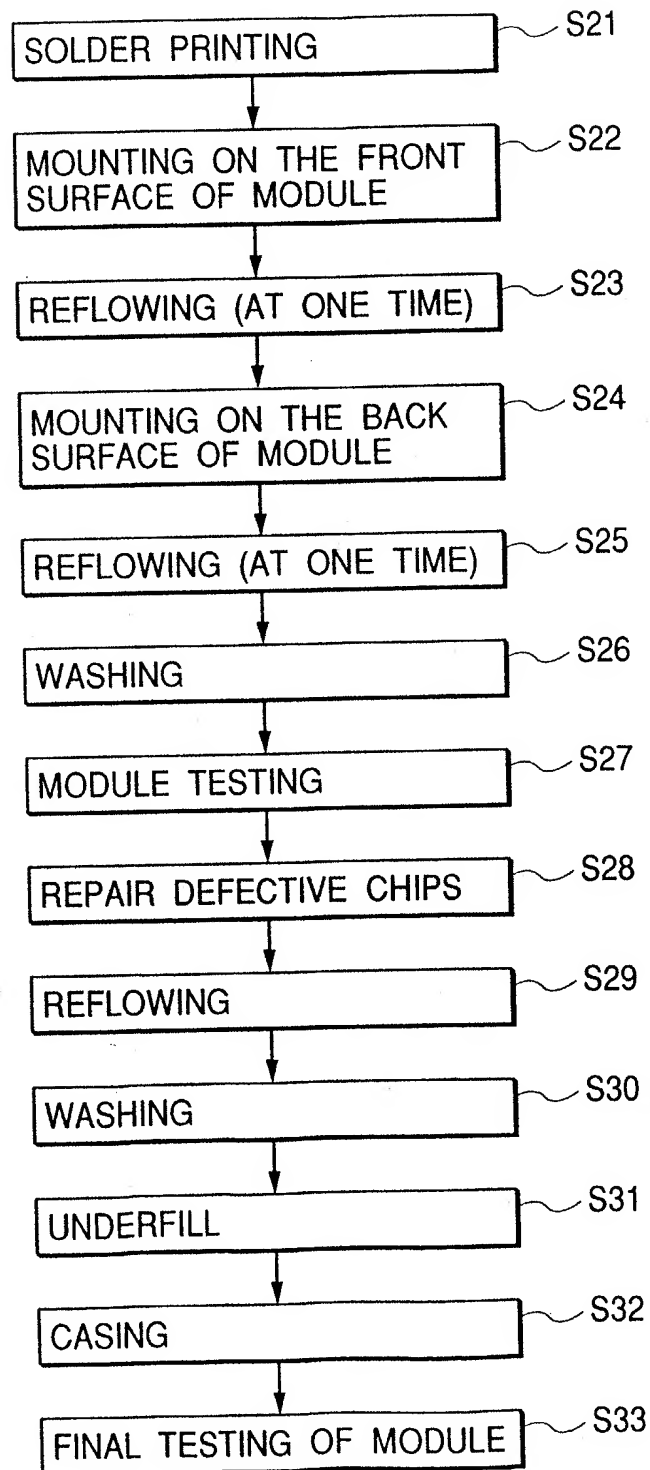
*FIG. 9*

FIG. 10

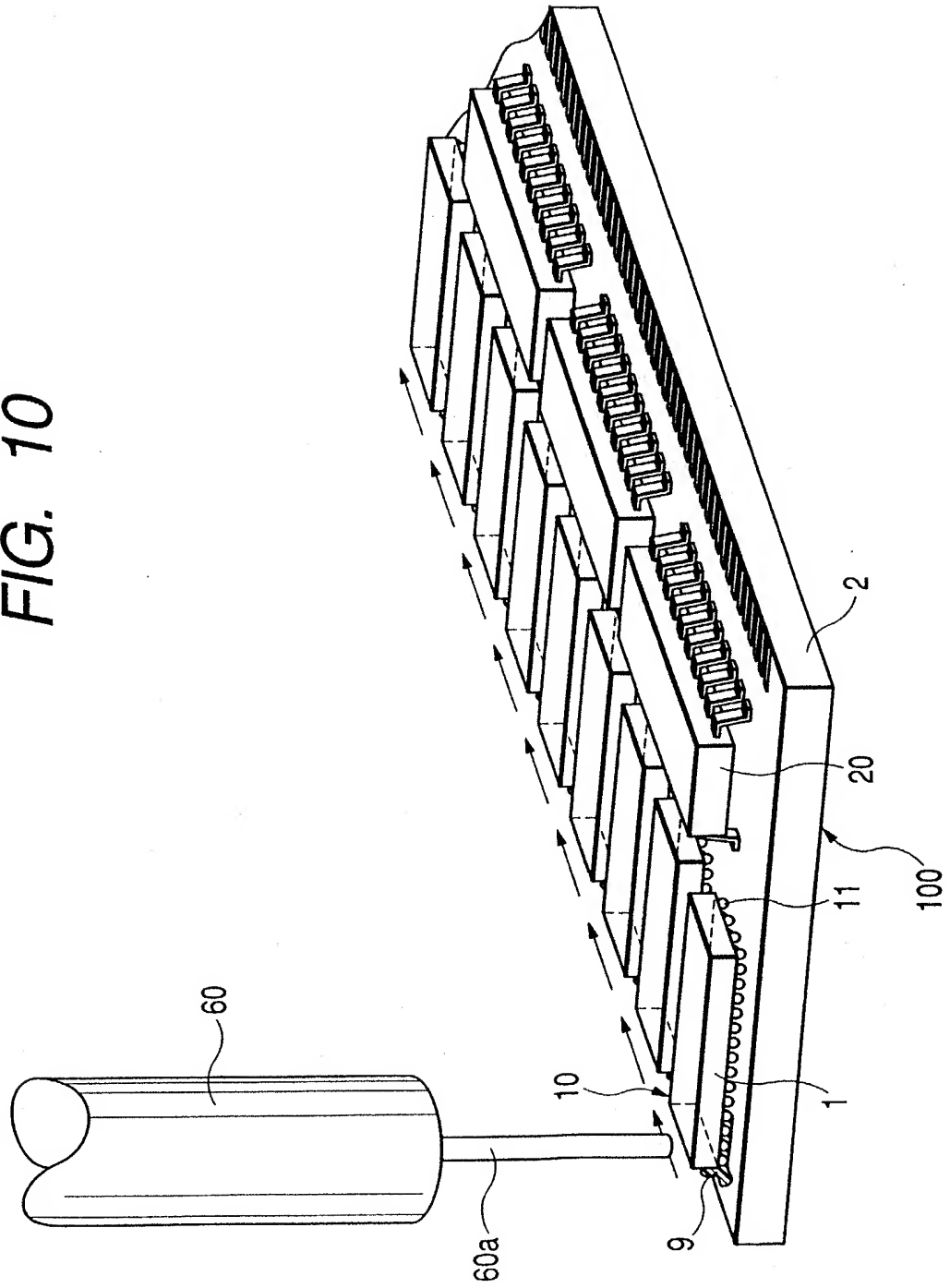


FIG. 11(a) FIG. 11(c) FIG. 11(e) FIG. 11(g)

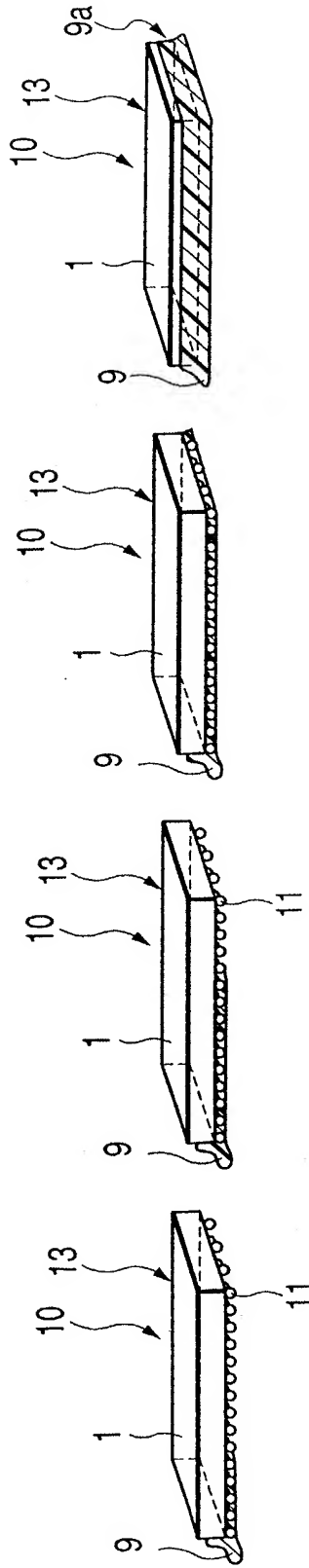
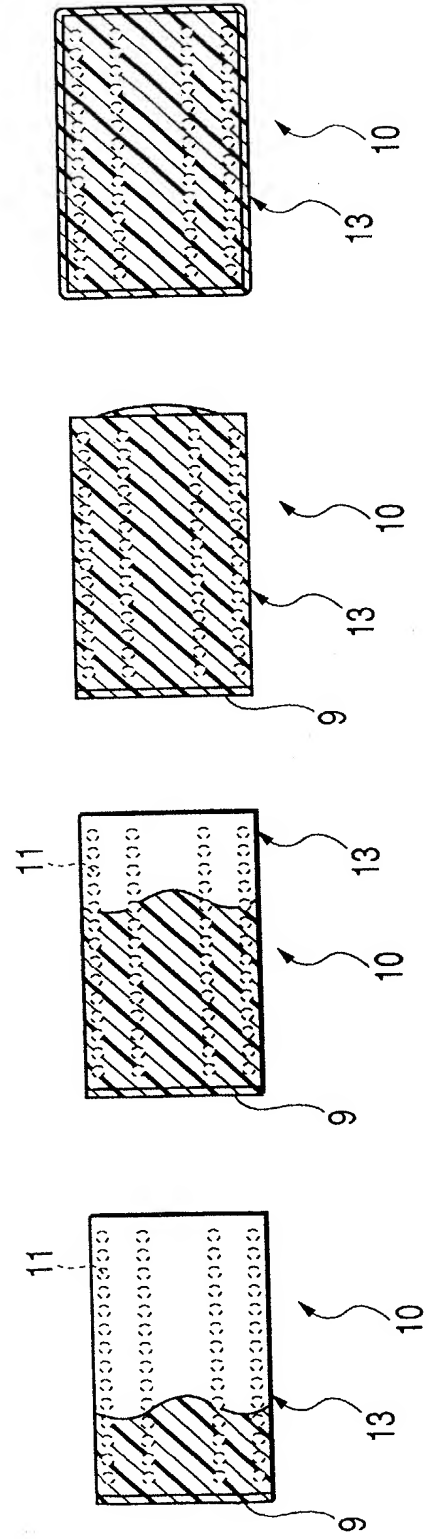


FIG. 11(b) FIG. 11(d) FIG. 11(f) FIG. 11(h)



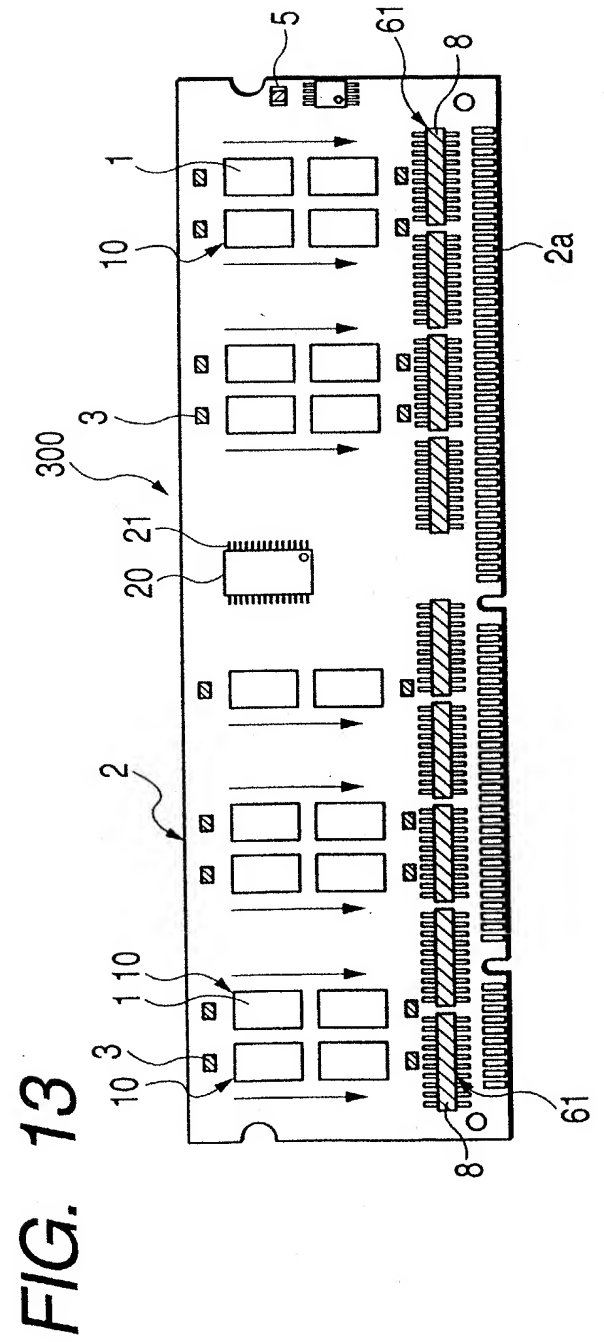
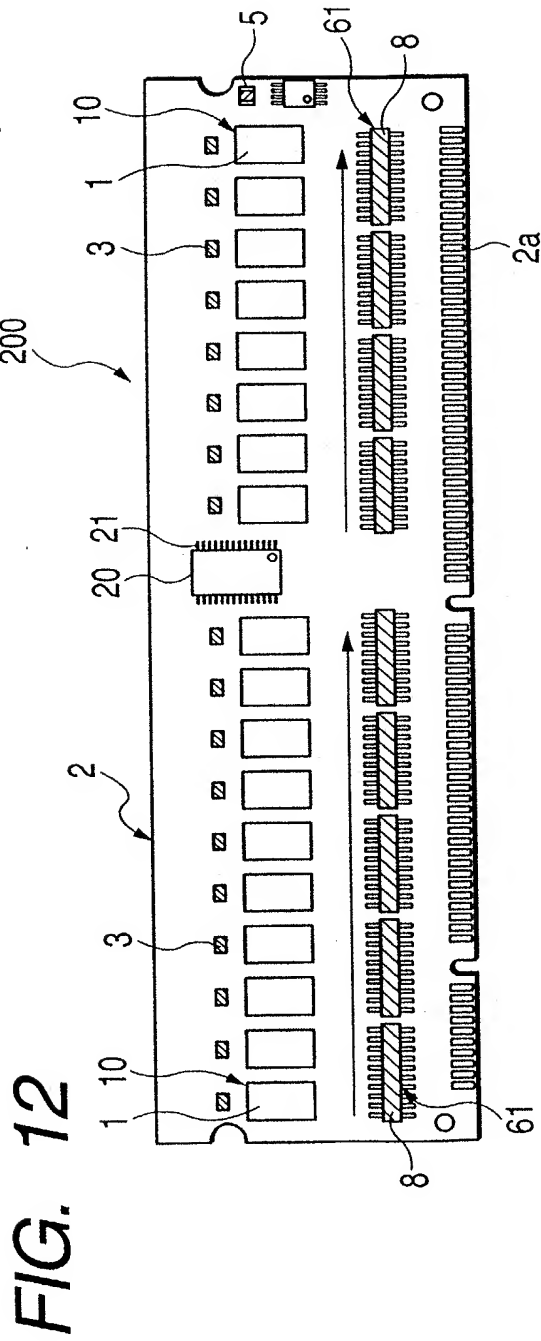


FIG. 14(a) FIG. 14(c) FIG. 14(e) FIG. 14(g)

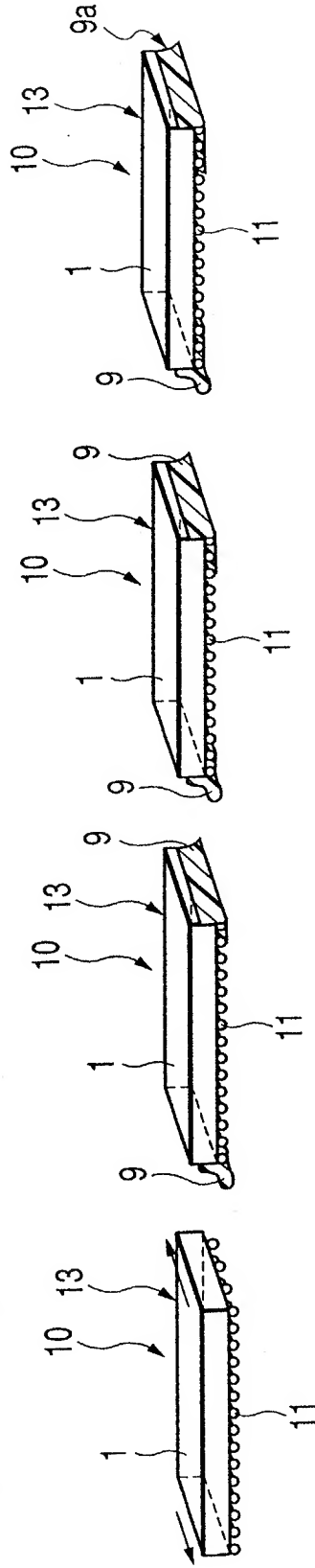


FIG. 14(b) FIG. 14(d) FIG. 14(f) FIG. 14(h)

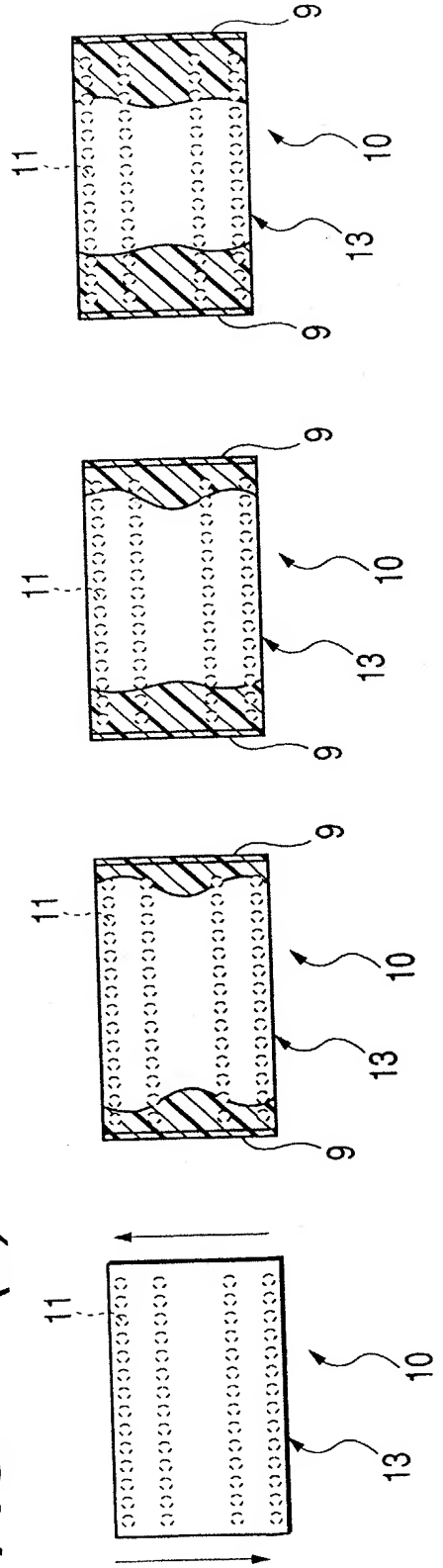


FIG. 15(a)

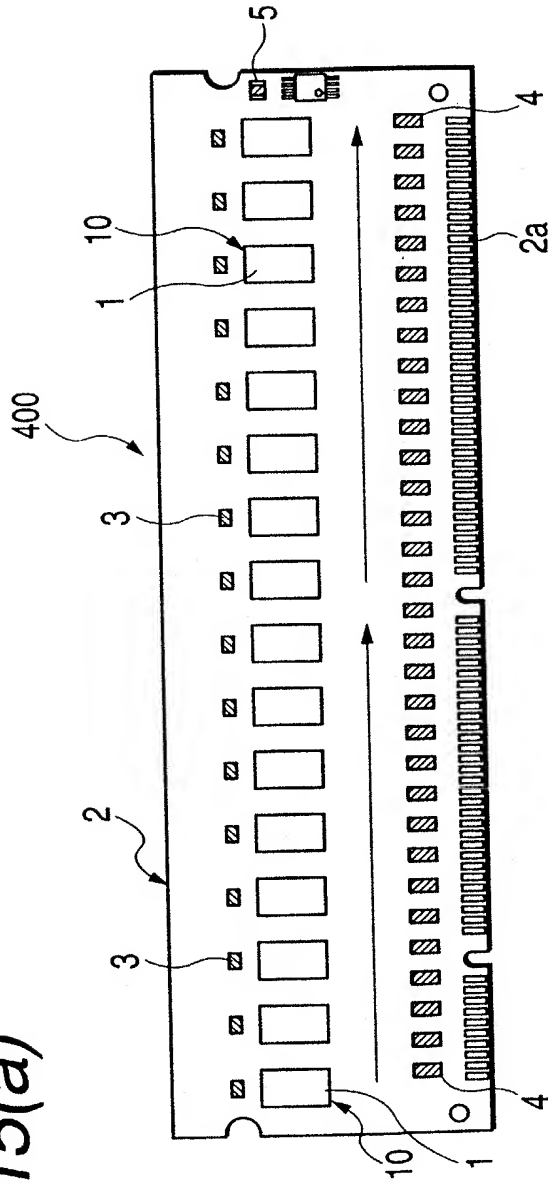
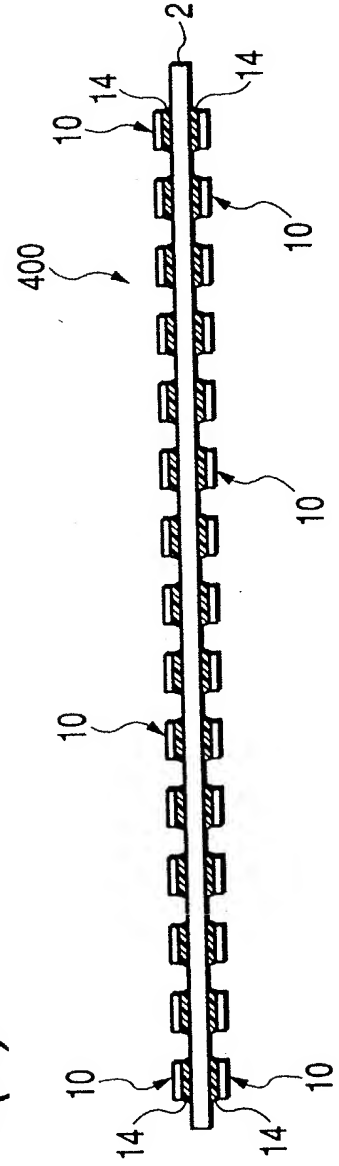
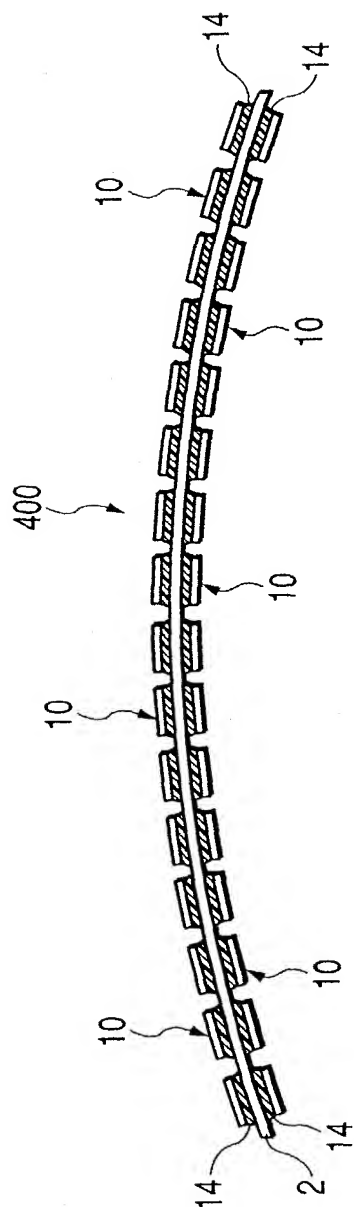


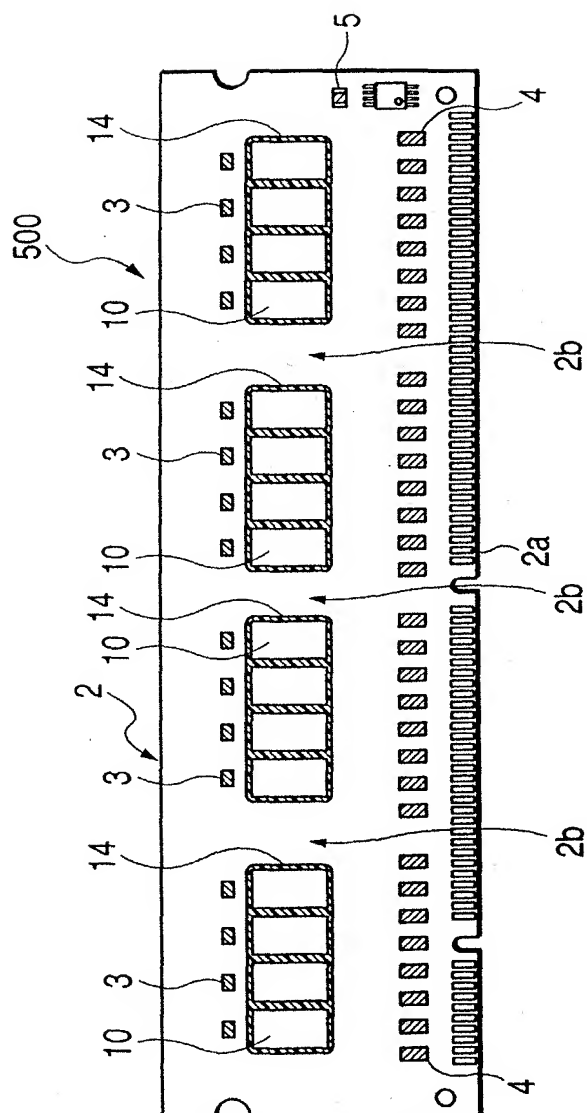
FIG. 15(b)



**FIG. 16**



**FIG. 17**



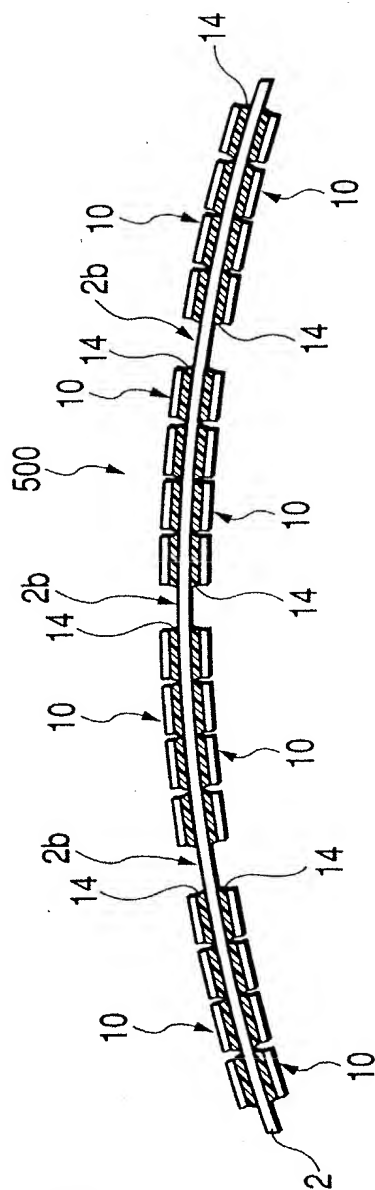


FIG. 18

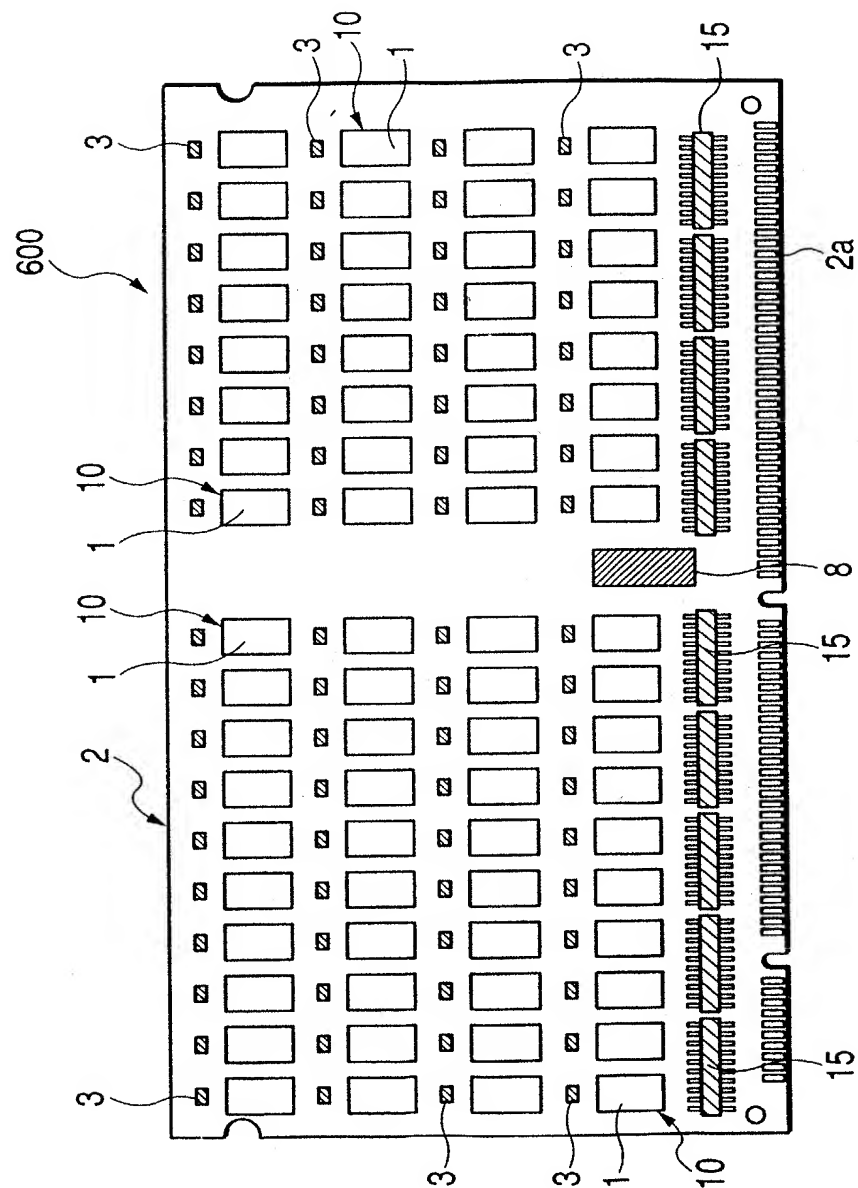


FIG. 19



FIG. 20(a)

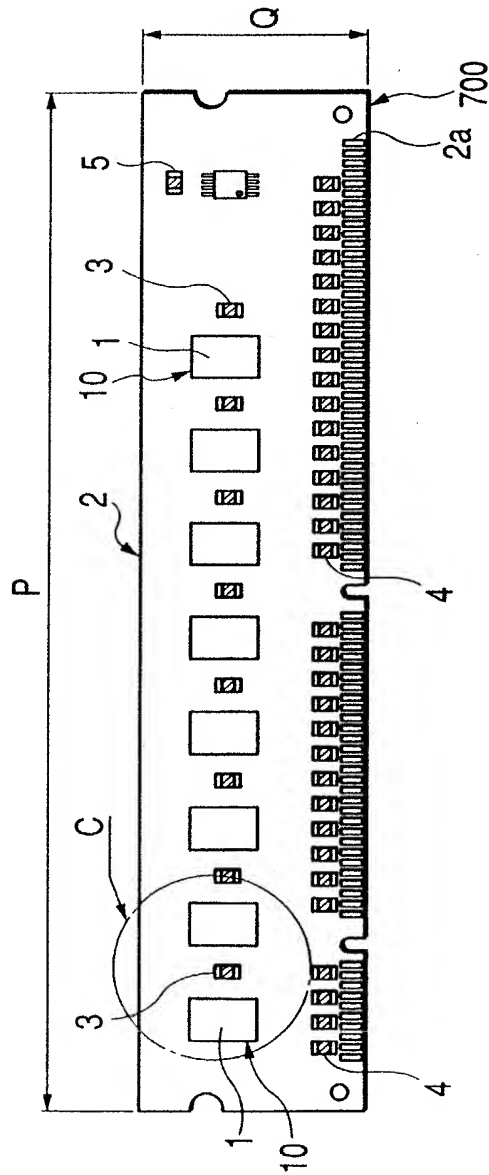
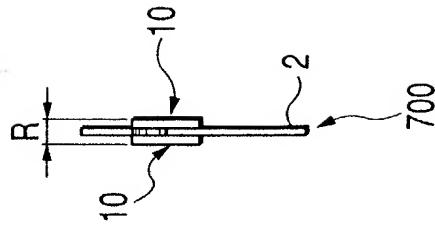


FIG. 20(b)





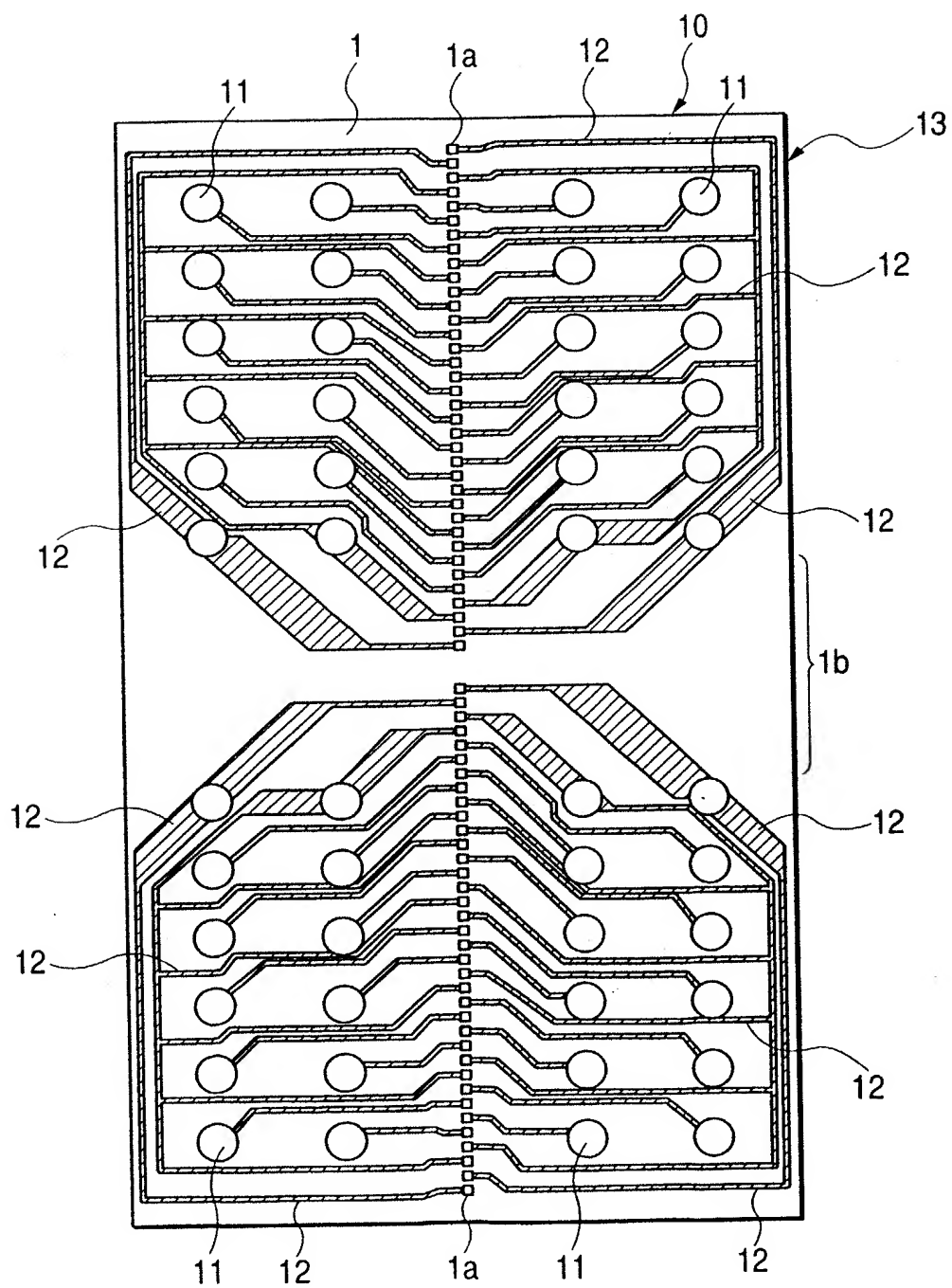
*FIG. 22*

FIG. 23

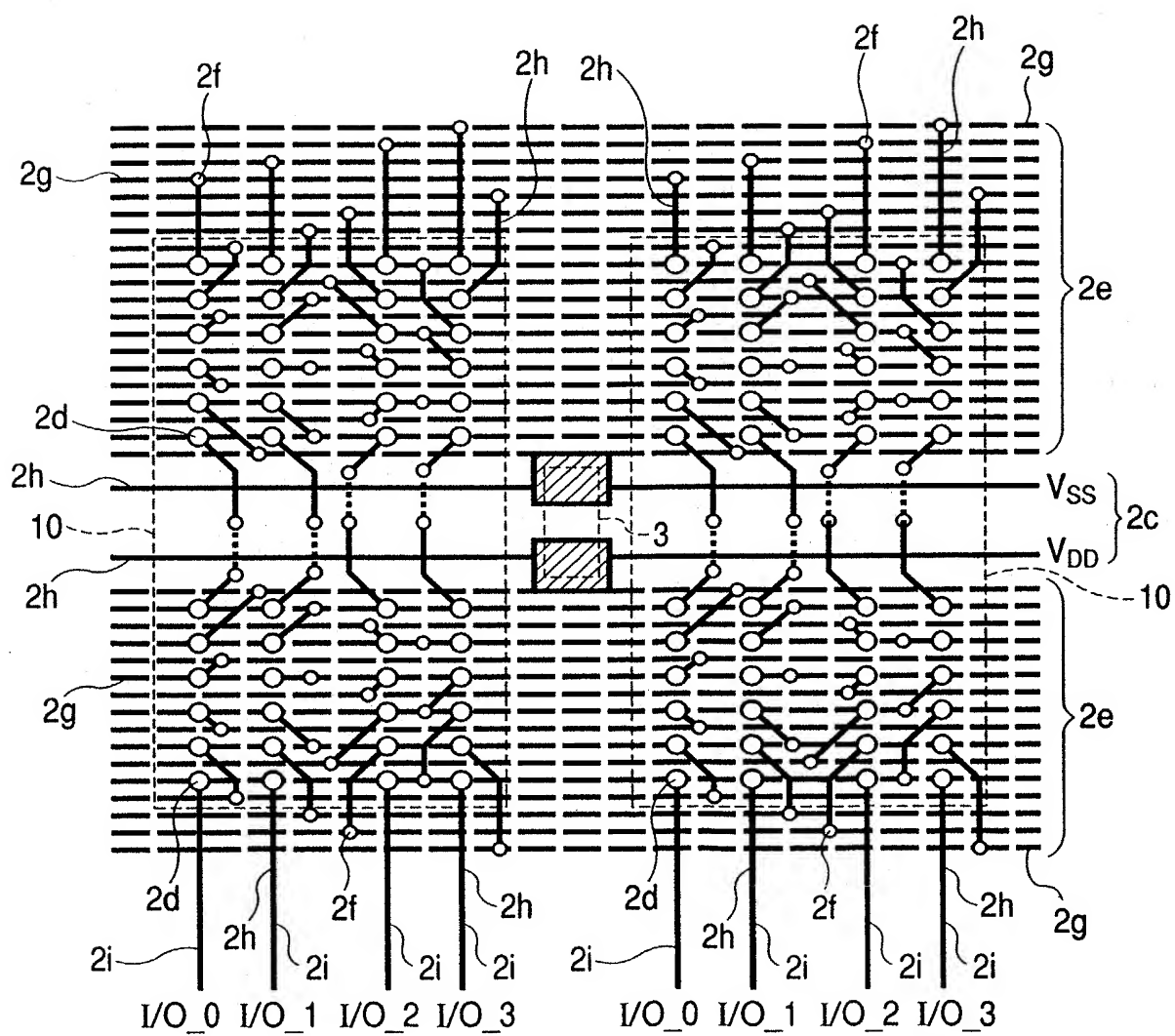


FIG. 24

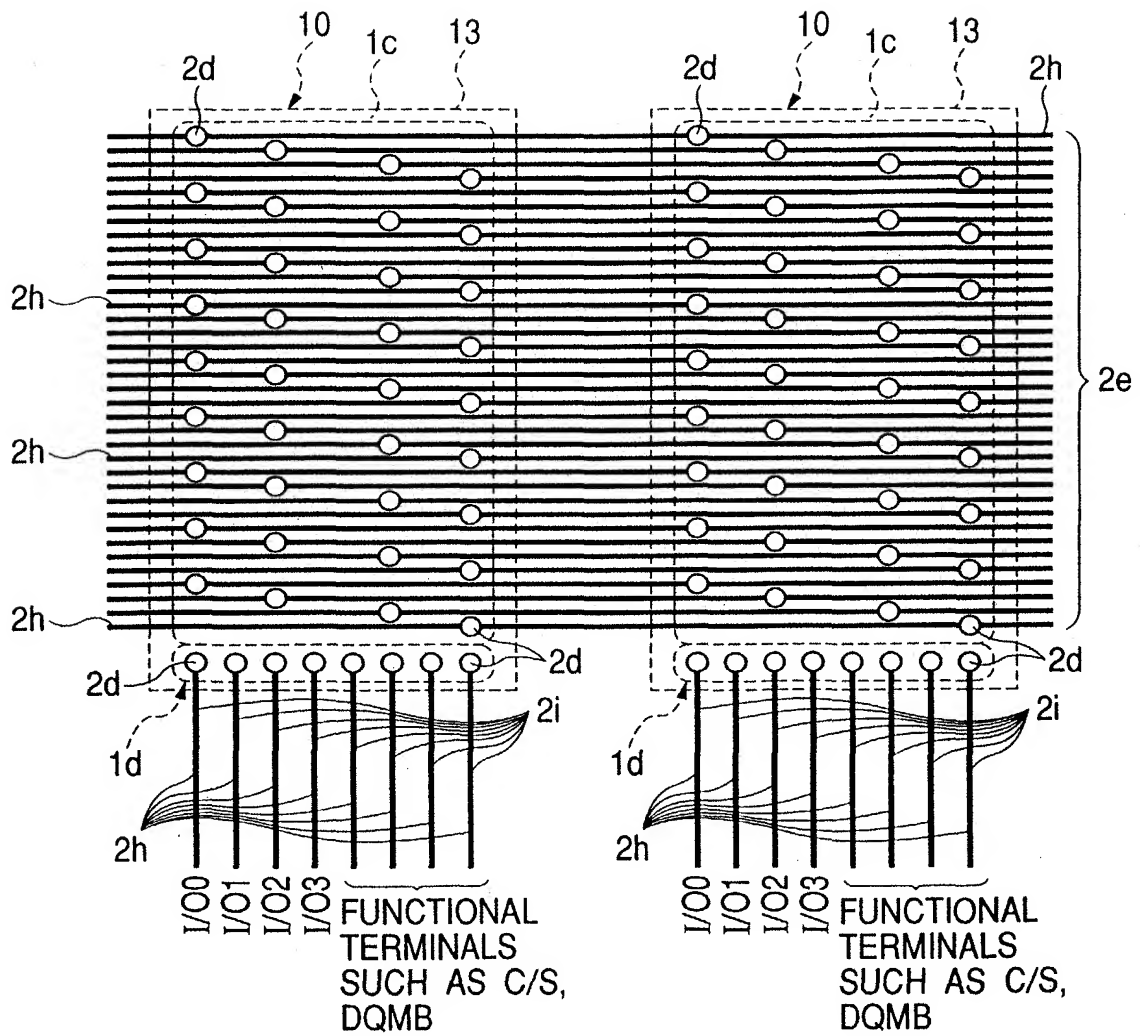


FIG. 25

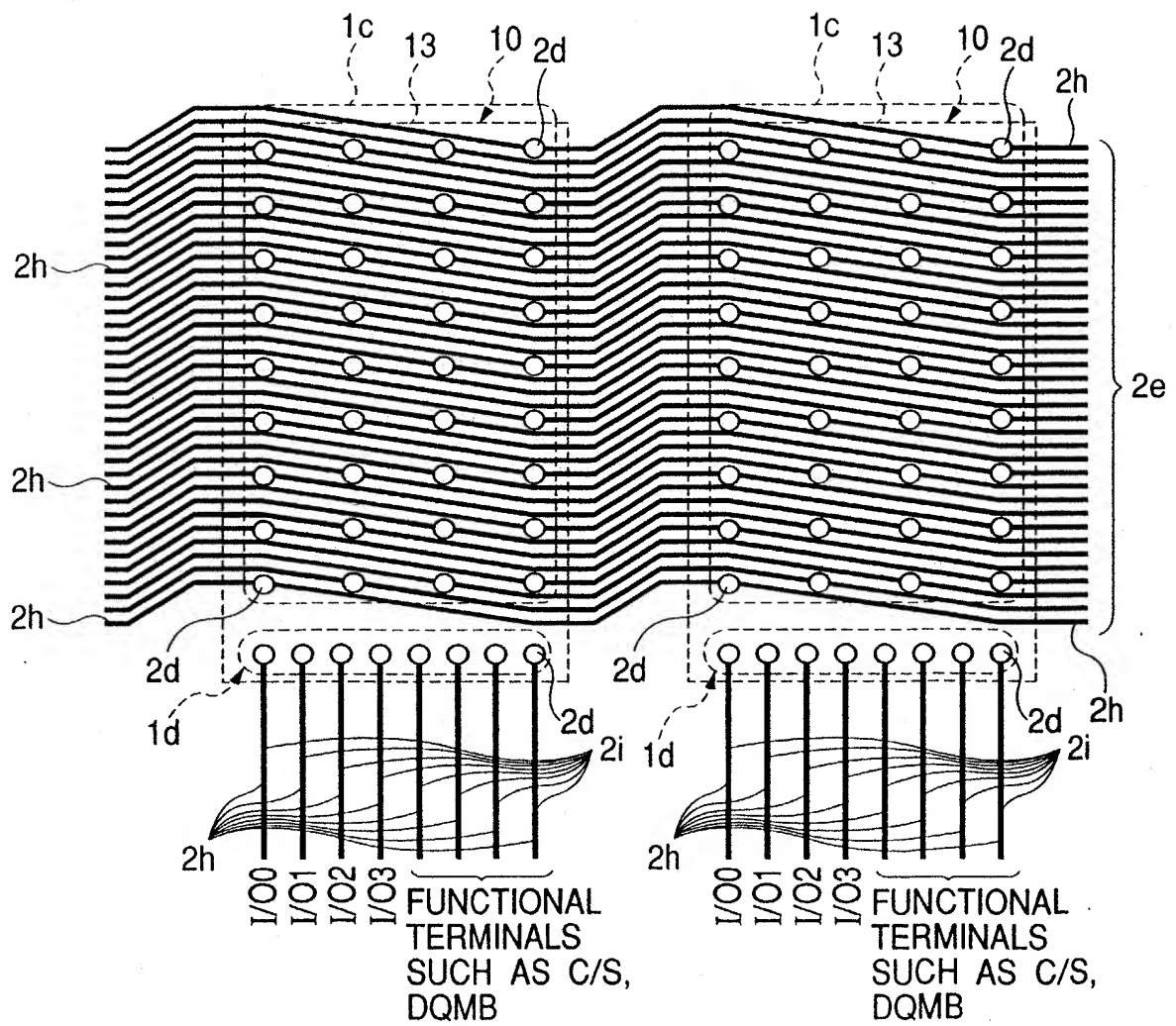
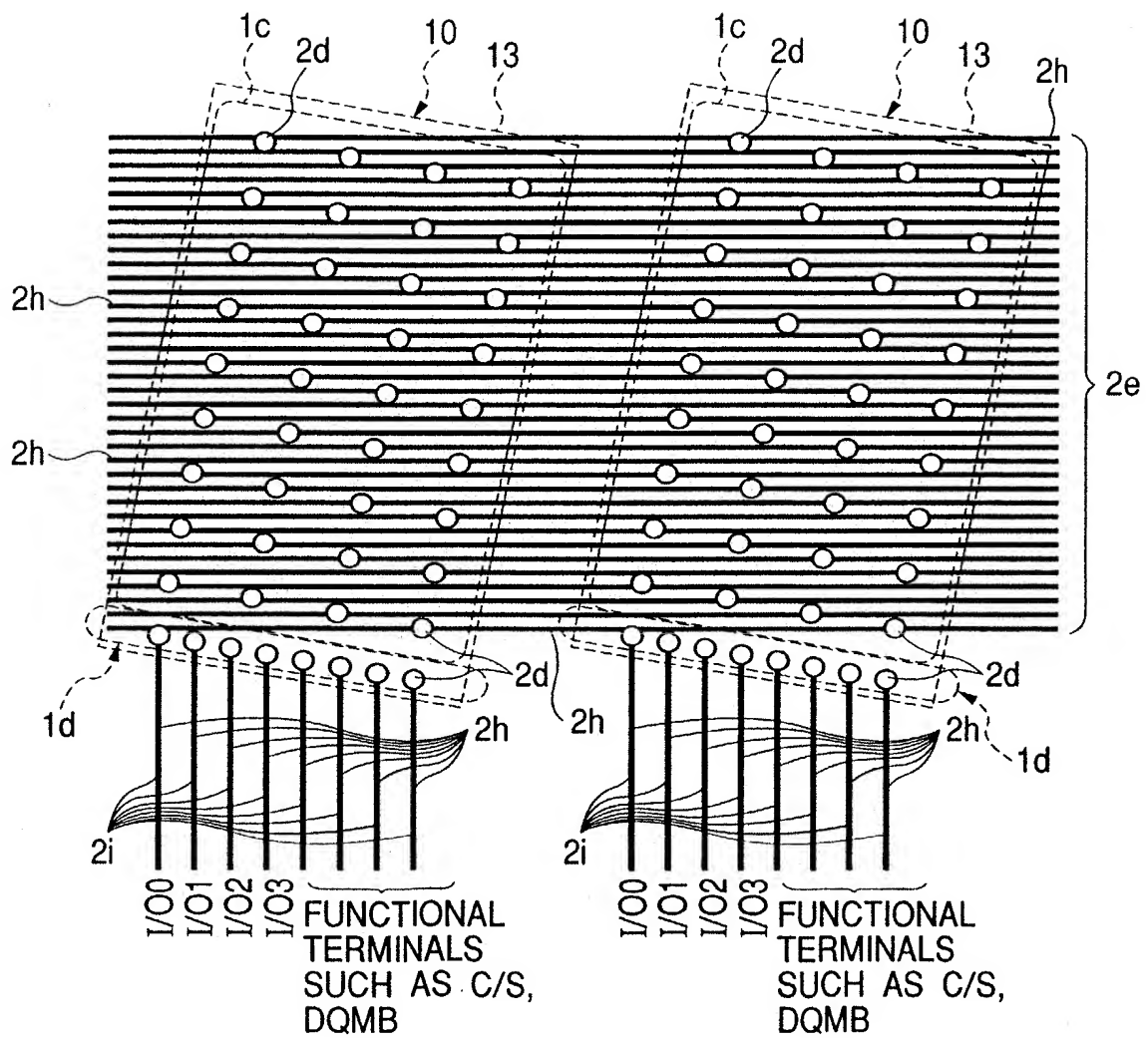


FIG. 26



The diagram shows a plan view of a semiconductor device with two symmetrical circuit blocks. Key features include:  
- Dimensions  $d_1$  and  $d_2$  indicating specific distances between components.  
- A central array of circular elements (vias or pads) arranged in rows and columns.  
- Conductive traces connecting these elements to peripheral pads labeled  $VDDQ$ ,  $VSSQ$ ,  $OVDD$ , and multiple  $I/O$  ports.  
- Dashed lines defining the boundaries of functional areas within each block.

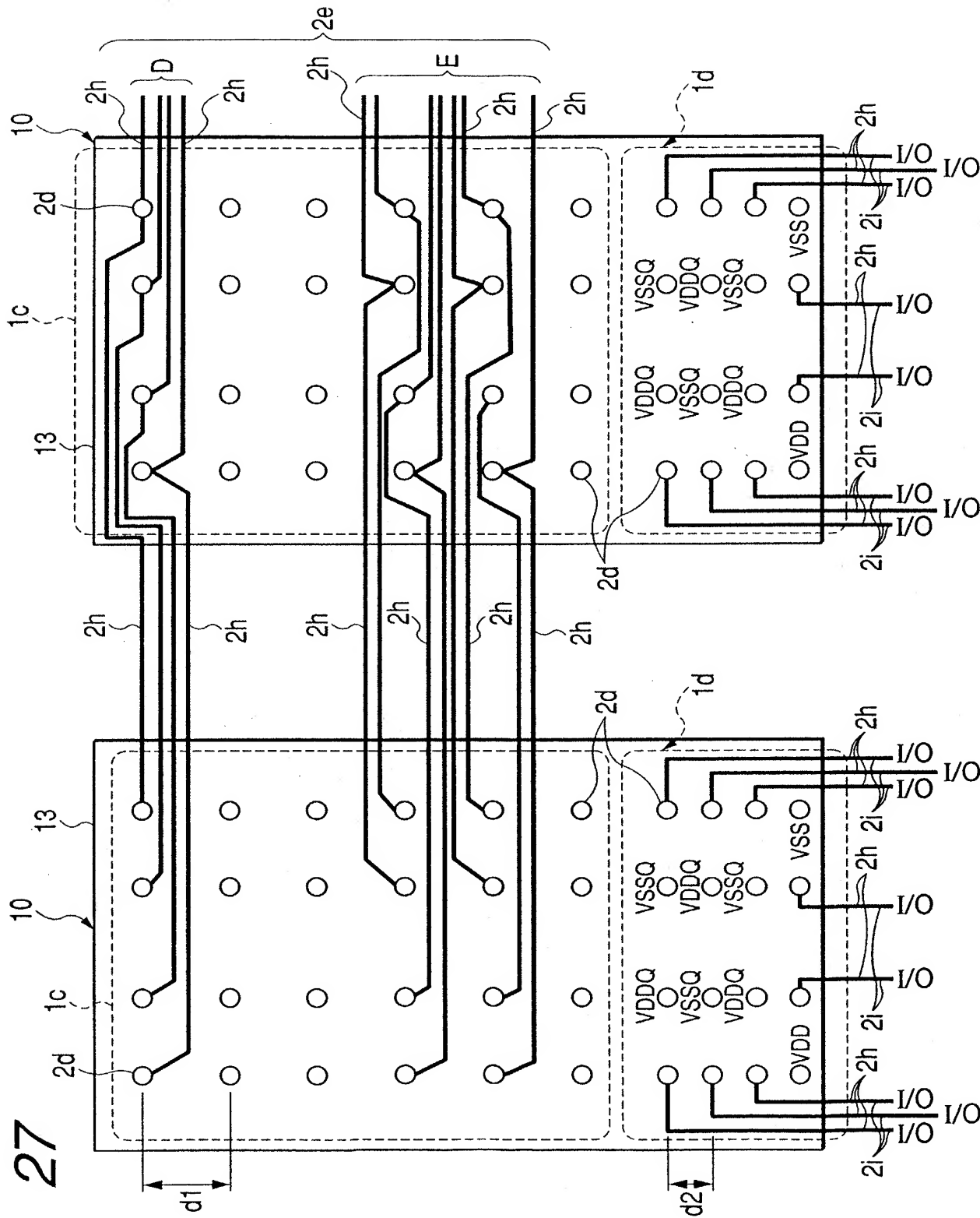




FIG. 28(a)

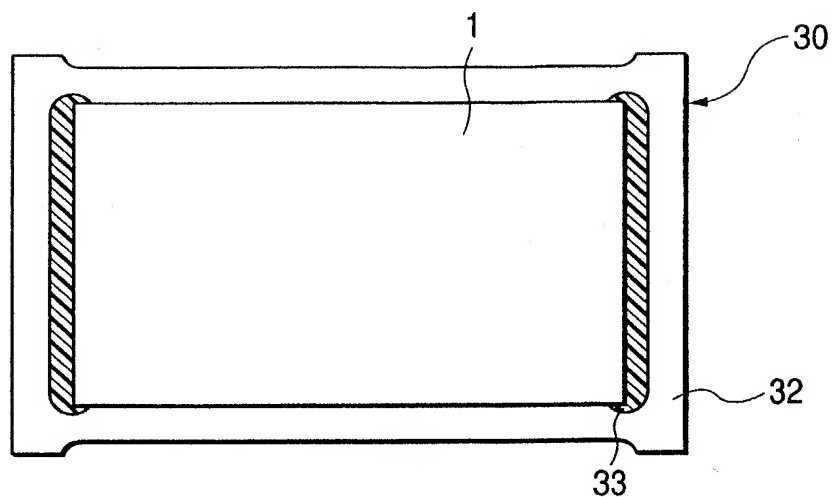


FIG. 28(b)

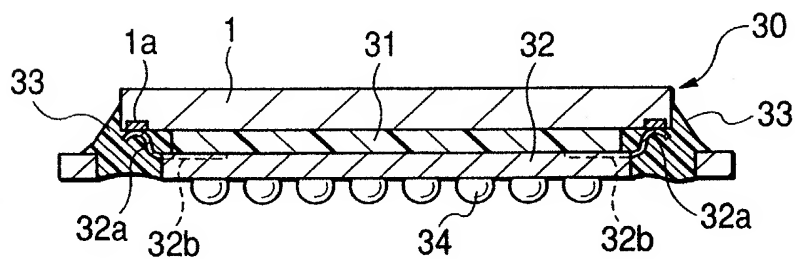
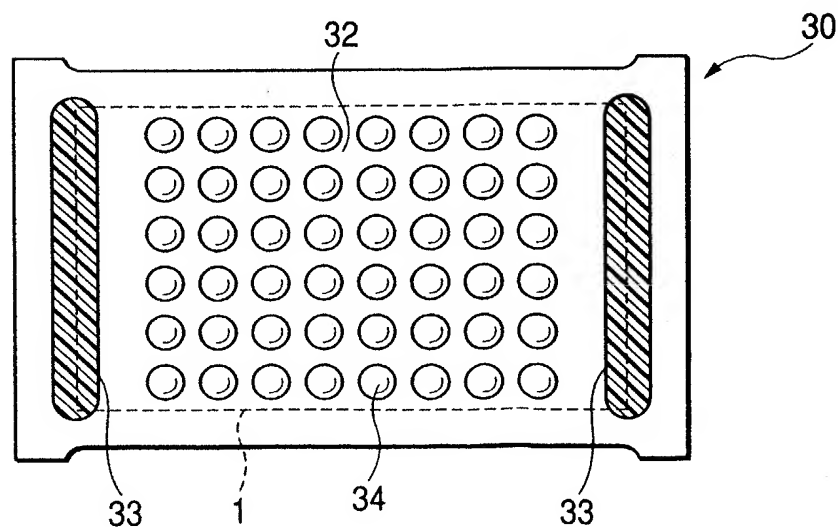


FIG. 28(c)



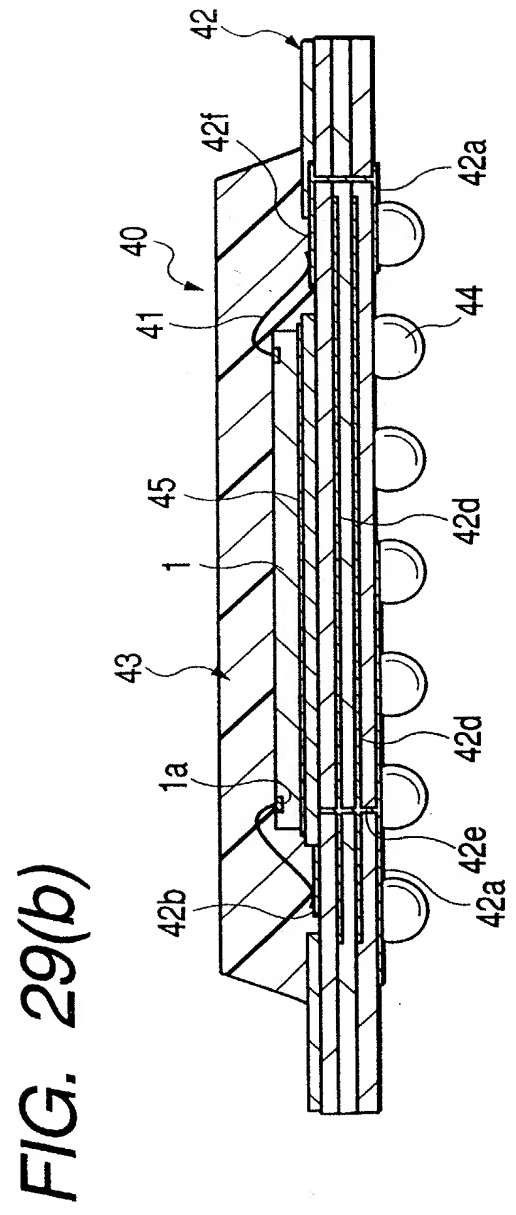
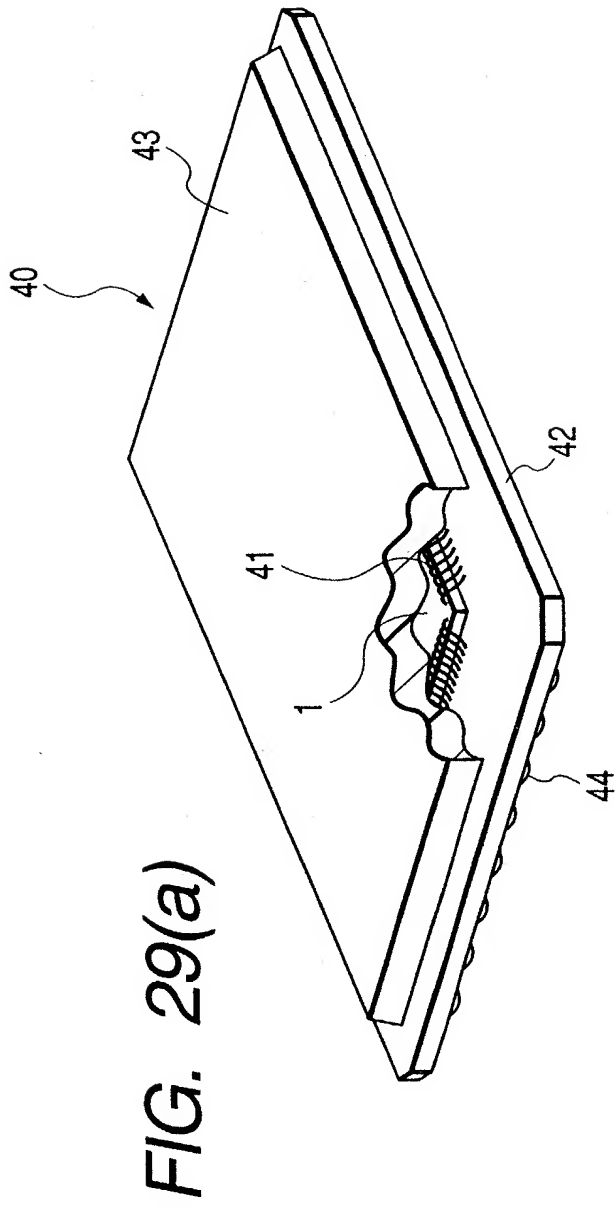


FIG. 30(a)

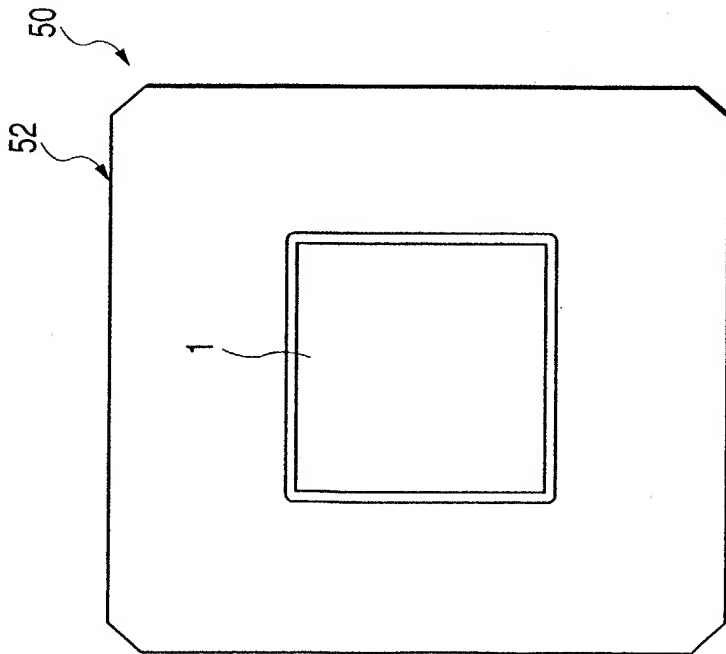


FIG. 30(c)

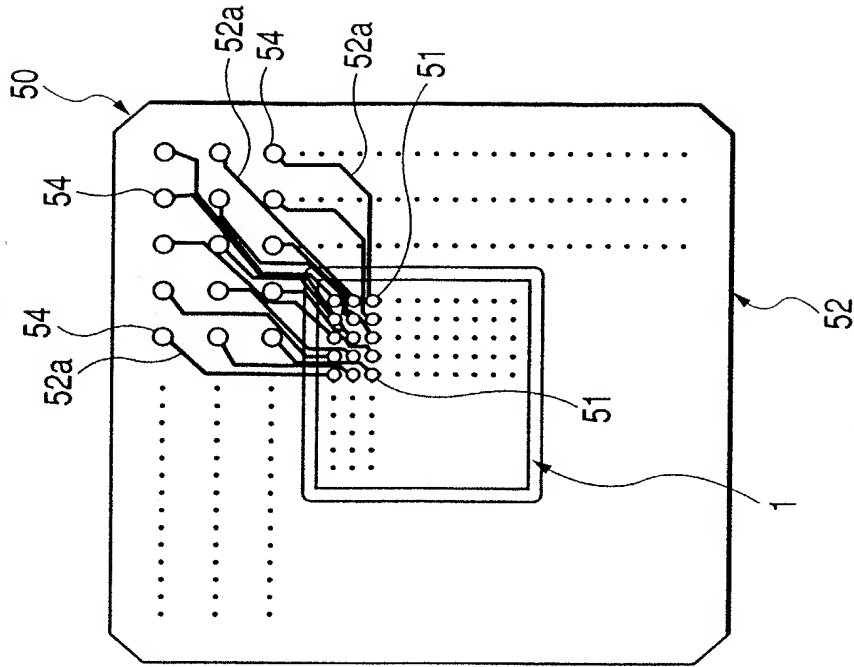


FIG. 30(b)

